Amendments to the Claims

This listing of the Claims will replace all prior versions and listings of the claims in this patent application.

Listing of the Claims

1-10. (canceled)

11. (currently amended) A method of forming an ~~chip scale~~electronic package ~~(CSP)~~ comprising the steps of:

separating a wafer into multiple dies;

after separating said wafer, joining at least one of said dies and a substrate, wherein multiple openings are formed in said substrate and expose said at least one of said dies;

depositing multiple solder balls into said openings; and

after said joining said at least one of said dies and said substrate, separating said substrate.

~~providing a first substrate and a first die, said first die joined with said first substrate;~~

~~using a testing fixture electrically connected to said first die;~~

~~providing a second substrate and a second die, said second die joined with said second substrate, said second substrate having a size identical to that of said first substrate, and said second die having a size different from that of said first die; and~~

~~using said test fixture electrically connected to said second die.~~

~~providing one or more chips having I/O pads with UBM layer on the surface of said I/O pads;~~

~~providing a substrate comprising bismaleimide triazine (BT) and having a thickness between about 150 to 300 μm;~~

~~applying an adhesive layer with a thickness between about 10 to 100 μm over said substrate, thus forming an adsubstrate composite;~~

~~forming openings in said adsubstrate composite to match the spacing of corresponding said I/O pads of said chip;~~

~~attaching said chip(s) on said adsubstrate composite wherein said I/O pads of said chip(s) are placed on the corresponding openings on said adsubstrate composite to form a package;~~

~~forming a molding material around said package;~~

~~performing ball mounting over said openings on said adsubstrate of said package; and~~

~~sawing said substrate to form said CSP.~~

12. (currently amended) The method of claim 11, further comprising depositing a UBM layer over multiple pads formed over an active surface of said wafer, followed by said separating said wafer, followed by said joining said at least one of said dies and said substrate, said UBM layer exposed by said openings in said substrate. ~~wherein said chip comprises silicon.~~

13. (currently amended) The method of claim 11, wherein- said openings are formed in said substrate before said joining said at least one of said dies and said substrate. ~~said I/O pads are area array (AA) type, or are redistributed to a redistribution layer to form AA I/O pads.~~

14. (canceled)

15. (currently amended) The method of claim 11, wherein said at least one of said dies comprises multiple pads and a passivation layer formed over an active surface thereof, said pads exposed by said openings in said substrate and exposed by multiple openings in said passivation layer. ~~said substrate comprises a Ball Grid Array (BGA).~~

16. (canceled)

17. (currently amended) The method of claim 11, wherein said at least one of said dies comprises multiple first pads, multiple second pads and a passivation layer formed over an active surface thereof, said first pads exposed by said openings in said substrate, said first pads deposited over said passivation layer, multiple openings formed in said passivation layer and exposing said second pads, said first pads electrically connected to said second pads, and said first pads having a layout different from that of said second pads. ~~said adhesive layer comprises polyimide thermocompression adhesive.~~

18. (canceled)

19. (currently amended) The method of claim 11, further comprising forming an adhesive material over said substrate, followed by said joining said at least one of said dies and said substrate using said adhesive material. ~~wherein said forming said openings is accomplished by mechanical or laser drilling, or screen printing.~~

20. (currently amended) The method of claim 11, after said joining said at least one of said dies and said substrate, further comprising forming a polymer layer encapsulating said at least one of said dies. ~~wherein said openings have a diameter between about 350 to 900 μm.~~

21. (currently amended) The method of claim 11, further comprising forming an adhesive material over said wafer, followed by said separating said wafer, followed by said joining said at least one of said dies and said substrate using said adhesive material. ~~wherein said attaching said chip(s) is accomplished by subjecting said adsubstrate to a temperature between about 250 and 350 °C at a pressure between about 1.5 to 2.5 Mpascals.~~

22. (currently amended) The method of claim ~~11~~21, wherein said depositing said adhesive layer over said wafer is performed using a process comprising spin coating, screen printing or lamination. ~~wherein said molding material comprises epoxy resin.~~

23. (currently amended) The method of claim 11, wherein- said substrate comprises bismaleimide triazine (BT). ~~said molding material has a thickness between about 100 to 500 μm.~~

24. (currently amended) The method of claim ~~11~~23, wherein said solder balls comprise tin-silver alloy.~~performing said ball mounting is accomplished with a solder comprising tin-lead or tin-silver alloy.~~

25. (currently amended) The method of claim 11, wherein said openings are formed using a process comprising mechanical drilling or laser drilling. ~~ball mountings have a height between about 300 to 800 μm.~~

26. (previously presented) A method of forming a chip scale package (CSP) comprising the steps of:

providing a wafer having a plurality of chip sites with I/O pads;

forming an under-ball metal (UBM) layer over said I/O pads;

forming an adhesive layer over said UBM layer on said wafer to form an adwafer;

forming openings in said adhesive layer on said adwafer to reach said I/O pads underlying said UBM layer;

thereafter die sawing said adwafer to form said chip scale package (CSP);

providing a substrate having openings corresponding to said I/O pads;

thereafter attaching said CSP with said adhesive to said substrate; and

thereafter forming ball mountings on said openings on said substrate to attach to said I/O pads on said CSP.

27. (original) The method of claim 26, wherein said wafer comprises silicon.

28. (original) The method of claim 26, wherein said I/O pads comprise aluminum alloy or copper.

29. (original) The method of claim 26, wherein said I/O pads are area array (AA) type, or redistributed to a redistribution layer to form AA pads.

30. (original) The method of claim 26, wherein said UBM layer comprises nickel and/or copper.

31. (original) The method of claim 26, wherein said forming said adhesive layer over said UBM layer comprises lamination, spin coating, or screen printing.

32. (original) The method of claim 26, wherein said adhesive layer comprises polyimide thermocompression advesive.

33. (canceled)

34. (original) The method of claim 26, wherein said forming said openings comprise laser drilling, photolithography, or silk screening.

35. (original) The method of claim 26, wherein said openings have a diameter between about 250 to 750 μm.

36. (original) The method of claim 26, wherein said substrate comprises bismaleimide triazine (BT) having a thickness between about 150 to 300 μm.

37. (previously presented) The method of claim 26, wherein said substrate comprises a Ball Grid Array (BGA).

38. (original) The method of claim 26, wherein said attaching said BGA substrate to said adhesive layer is accomplished at a temperature between about 250 and 350 °C, and pressure between about 1.5 to 2.5 Mpascals.

39. (original) The method of claim 26, wherein said ball mountings comprise solder having a composition lead-tin or tin-silver.

40. (original) The method of claim 26, wherein said mounting balls have a height between about 300 to 800 μm.

41. (original) The method of claim 26, wherein said CSP is encapsulated in a molding material comprising epoxy resin.

42. (currently amended) A method of forming ~~a chip scale~~ an electronic package ~~(CSP)~~ comprising the steps of:

~~or more chips having I/O pads with UBM layer on the surface of said I/O pads;~~

depositing an adhesive material over a substrate; and

after said depositing said adhesive layer, joining at least a die and said substrate using said adhesive layer, wherein multiple openings are formed in said substrate and expose said die.

~~providing a substrate comprising bismaleimide triazine (BT) and having a thickness between 150 to 300 μm;~~

~~applying an adhesive layer with a thickness between 10 to 100 μm over said substrate, thus forming an adsubstrate composite;~~

~~forming openings in said adsubstrate composite to match the spacing of corresponding said I/O pads of said chip;~~

~~attaching said chip(s) on said adsubstrate composite wherein said I/O pads of said chip(s) are placed on the corresponding openings on said adsubstrate composite to form a package wherein said attaching is accomplished by subjecting said adsubstrate to a temperature of between 250 and 350 °C at a pressure of between 1.5 to 2.5 Mpascals;~~

~~forming a molding material around said package;~~

~~thereafter performing ball mounting over said openings on said adsubstrate of said package; and~~

~~sawing said substrate to form said CSP.~~

43. (currently amended) The method of claim 42, wherein said die comprises a UBM layer exposed by said openings. ~~wherein said chip comprises silicon~~.

44. (currently amended) The method of claim 42 wherein said openings in said substrate expose multiple pads exposed by multiple openings in a passivation layer formed over an active surface of said die. ~~said I/O pads are area array (AA) type, or are redistributed to a redistribution layer to form AA I/O pads.~~

45. (currently amended) The method of claim 42 wherein said openings in said substrate expose multiple first pads deposited over a passivation layer formed over an active surface of said die, wherein multiple openings are formed in said passivation layer and expose multiple second pads formed over said active surface of said die, said first pads electrically connected to said second pads, and said first pads having a layout different from that of said second pads. ~~substrate comprises a Ball Grid Array (BGA).~~

46. (currently amended) The method of claim 42, after said joining said die and said substrate, further comprising forming a polymer layer encapsulating said die. ~~wherein said adhesive layer comprises polyimide thermocompression adhesive~~.

47. (currently amended) The method of claim 42, after joining said die and said substrate, further comprising separating said substrate. ~~wherein said forming said openings is accomplished by mechanical or laser drilling or screen printing~~.

48. (currently amended) The method of claim 42, wherein said openings are formed in said substrate before said joining said die and said substrate. ~~wherein said openings have a diameter between about 350 and 900 μm~~.

49. (currently amended) The method of claim 42, wherein said substrate comprises bismaleimide triazine (BT). ~~wherein said molding material comprises epoxy resin~~.

50. (currently amended) The method of claim 42, after said joining said die and said substrate, further comprising depositing a conductive material into said openings ~~wherein said performing said ball mounting is accomplished with a solder comprising tin-lead or tin-silver alloy~~.

51. (currently amended) The method of claim ~~50~~, 50, wherein said conductive material comprises multiple solder balls. ~~42 wherein said ball mountings have a height between about 300 and 800 μm~~.

52. (new) A method of forming an electronic package comprising the steps of:

providing at least a die comprising a UBM layer; and

joining said die and a substrate, wherein multiple openings are formed in said substrate and expose said UBM layer.

53. (new) The method of claim 52, after said joining said die and said substrate, further comprising depositing a conductive material into said openings.

54. (new) The method of claim 53, wherein said conductive material comprises multiple solder balls.

55. (new) The method of claim 52, wherein said die comprises multiple pads exposed by multiple openings in a passivation layer formed over an active surface of said die, said UBM layer formed over said pads.

56. (new) The method of claim 52, wherein said die comprises a passivation layer and a metal layer formed over an active surface thereof, said metal layer deposited over said passivation layer, said UBM layer deposited over said metal layer.

57. (new) The method of claim 52, after said joining said die and said substrate, further comprising separating said substrate.

58. (new) The method of claim 52, after said joining said die and said substrate, further comprising forming a polymer layer encapsulating said die.

59. (new) The method of claim 52, further comprising depositing an adhesive material over said die, followed by said joining said die and said substrate using said adhesive material.

60. (new) The method of claim 52, further comprising depositing an adhesive material over said substrate, followed by said joining said die and said substrate using said adhesive material.

61. (new) The method of claim 52, wherein said openings are formed in said substrate before said joining said die and said substrate.

62. (new) The method of claim 52, wherein said UBM layer comprises copper or nickel.

63. (new) A method of forming an electronic package comprising the steps of:

joining at least a die and a substrate, wherein multiple openings are formed in said substrate and expose said die; and

depositing a conductive material into said openings, wherein said conductive material is suited for connecting said die to an external circuitry.

64. (new) The method of claim 63, wherein said conductive material comprises multiple solder balls.

65. (new) The method of claim 63, wherein said conductive material comprises tin-lead alloy or tin-silver alloy.

66. (new) The method of claim 63, wherein said external circuitry comprises a next level of packaging.

67. (new) The method of claim 63, wherein said die comprises a UBM layer and multiple pads formed over an active surface thereof, said UBM layer formed over said pads, and said UBM layer exposed by said openings in said substrate.

68. (new) The method of claim 63, wherein said die comprises multiple pads exposed by said openings in said substrate and exposed by multiple openings in a passivation layer formed over an active surface of said die.

69. (new) The method of claim 63, wherein said die comprises multiple pads, a passivation layer and a metal layer formed over an active surface thereof, said passivation layer exposing said pads, said metal layer deposited over said passivation layer and electrically connected to said pads, and said openings exposing said metal layer.

70. (new) The method of claim 63, after said depositing said conductive material, further comprising separating said substrate.

71. (new) The method of claim 63, after said joining said die and said substrate, further comprising forming a polymer layer encapsulating said die.

72. (new) The method of claim 63, further comprising forming an adhesive material over said die, followed by said joining said die and said substrate using said adhesive material.

73. (new) The method of claim 63, further comprising forming an adhesive material over said substrate, followed by said joining said die and said substrate using said adhesive material.

74. (new) The method of claim 63, wherein said openings are formed in said substrate before said joining said die and said substrate.

75. (new) A method of forming an electronic package comprising the steps of:

depositing an adhesive material over an active surface of a die; and

after said depositing said adhesive material, joining said die and a carrier using said adhesive material.

76. (new) The method of claim 75, after said joining said die and said carrier, further comprising separating said carrier.

77. (new) The method of claim 75, wherein multiple first openings are formed in said adhesive material and expose a metal layer formed over said active surface of said die.

78. (new) The method of claim 77, wherein said first openings are formed using a process comprising laser drilling or photolithography.

79. (new) The method of claim 77, wherein said first openings are formed after said depositing said adhesive material over said active surface of said die.

80. (new) The method of claim 77, wherein said first openings are formed during said depositing said adhesive material over said active surface of said die.

81. (new) The method of claim 77, wherein said die comprises multiple pads and a passivation layer formed over said active surface thereof, said passivation layer having multiple second openings exposing said pads, said metal layer deposited over said passivation layer and electrically connected to said pads.

82. (new) The method of claim 77, after said joining said die and said carrier, further comprising depositing a conductive material into multiple second openings in said carrier and into said first openings, said first and second openings being aligned and exposing said metal layer.

83. (new) The method of claim 82, wherein said conductive material comprises multiple solder balls.

84. (new) The method of claim 82, wherein said second openings are formed before said joining said die and said carrier.

85. (new) The method of claim 75, after said joining said die and said carrier, further comprising forming a polymer layer encapsulating said die.

86. (new) The method of claim 75, wherein said adhesive material is deposited using a process comprising spin coating, screen printing or lamination.

87. (new) The method of claim 75, wherein the step of said depositing said adhesive material comprises depositing said adhesive material over a wafer comprising a plurality of said dies and separating said wafer into a plurality of said dies over which said adhesive material is deposited.

88. (new) The method of claim 75, wherein said carrier comprises a substrate.

89. (new) A method of forming an electronic package comprising the steps of:

depositing an adhesive material over a die, wherein at least an opening is formed in said adhesive material and exposes said die; and

after said depositing said adhesive material, joining said die and a carrier using said adhesive material.

90. (new) The method of claim 89, after said joining said die and said carrier, further comprising separating said carrier.

91. (new) The method of claim 89, wherein said opening is formed using a process comprising laser drilling or photolithography.

92. (new) The method of claim 89, wherein said opening is formed after said depositing said adhesive material over said die.

93. (new) The method of claim 89, wherein said opening is formed during said depositing said adhesive material over said die.

94. (new) The method of claim 89, after said joining said die and said carrier, further comprising depositing a conductive material into at least an opening in said carrier and into said opening in said adhesive material, said opening in said carrier being aligned with said opening in said adhesive material.

95. (new) The method of claim 94, wherein said conductive material comprises at least a solder ball.

96. (new) The method of claim 94, wherein said opening in said carrier is formed before said joining said die and said carrier.

97. (new) The method of claim 89, after said joining said die and said carrier, further comprising forming a polymer layer encapsulating said die.

98. (new) The method of claim 89, wherein said adhesive material is deposited using a process comprising spin coating, screen printing or lamination.

99. (new) The method of claim 89, wherein the step of said depositing said adhesive material comprises depositing said adhesive material over a wafer comprising a plurality of said dies and separating said wafer into a plurality of said dies over which said adhesive material is deposited.

100. (new) The method of claim 89, wherein said carrier comprises a substrate.

101. (new) The method of claim 89, wherein the number of said openings is multiple.

102. (new) A method of forming an electronic package comprising the steps of:

depositing a UBM layer over a wafer;

separating said wafer into multiple dies;

joining at least one of said dies and a substrate, wherein multiple openings are formed in said substrate and expose said UBM layer; and

depositing a conductive material over said UBM layer exposed by said openings.

103. (new) The method of claim 102, wherein said conductive material comprises at least a solder ball.

104. (new) The method of claim 102, wherein said UBM layer is deposited over multiple pads exposed by multiple openings in a passivation layer formed over an active surface of said wafer.

105. (new) The method of claim 102, wherein said wafer comprises multiple pads, a passivation layer and a metal layer formed over an active surface thereof, said passivation layer exposing said pads, said metal layer deposited over said passivation layer and electrically connected to said pads, and said UBM layer deposited over said metal layer.

106. (new) The method of claim 102, after said depositing said conductive material, further comprising separating said substrate.

107. (new) The method of claim 102, after joining said at least one of said dies and said substrate, further comprising forming a polymer layer encapsulating at least one of said dies.

108. (new) The method of claim 102, further comprising forming an adhesive material over said wafer, followed by said separating said wafer, followed by said joining at least one of said dies and said substrate using said adhesive material.

109. (new) The method of claim 102, further comprising forming an adhesive material over said substrate, followed by said joining at least one of said dies and said substrate using said adhesive material.

110. (new) The method of claim 102, wherein said opening is formed in said substrate before said joining at least one of said dies and said substrate.

111. (new) The method of claim 102, wherein said UBM layer comprises copper or nickel.

112. (new) A method of forming an electronic package comprising the steps of:

depositing an adhesive material over a die; and

after said depositing said adhesive material, joining said die and a substrate using said adhesive material.

113. (new) The method of claim 112, after said joining said die and said substrate, further comprising separating said substrate.

114. (new) The method of claim 112, after said joining said die and said substrate, further comprising forming a polymer layer encapsulating said die.

115. (new) The method of claim 112, wherein said adhesive material is deposited using a process comprising spin coating, screen printing or lamination.

116. (new) The method of claim 112, wherein the step of said depositing said adhesive material comprises depositing said adhesive material over a wafer comprising a plurality of said dies and separating said wafer into a plurality of said dies over which said adhesive material is deposited.

117. (new) A method of forming an electronic package comprising the steps of:

providing a die comprising a passivation layer and a metal layer, said metal layer formed over said passivation layer; and

joining said die and a substrate, wherein multiple openings are formed in said substrate and expose said metal layer.

118. (new) The method of claim 117, wherein said openings are formed in said substrate before said joining said die and said substrate.

119. (new) The method of claim 117, wherein said metal layer comprises a UBM layer exposed by said openings.

120. (new) The method of claim 119, wherein said UBM layer comprises copper or nickel.

121. (new) The method of claim 117, after said joining said die and said substrate, further comprising forming a polymer layer encapsulating said die.

122. (new) The method of claim 117, further comprising forming an adhesive material over said die, followed by said joining said die and said substrate using said adhesive material.

123. (new) The method of claim 117, further comprising forming an adhesive material over said substrate, followed by said joining said die and said substrate using said adhesive material.

124. (new) The method of claim 117, after said joining said die and said substrate, further comprising depositing a conductive material into said openings.

125. (new) The method of claim 124, wherein said conductive material comprises multiple solder balls.

126. (new) The method of claim 117, wherein said die further comprises multiple pads exposed by multiple openings in said passivation layer, said metal layer electrically connected to said pads.

127. (new) A method of forming an electronic package comprising the steps of:

providing a die comprising multiple pads and a passivation layer, multiple openings formed in said passivation layer and exposing said pads; and

joining said die and a substrate, multiple openings formed in said substrate and exposing said pads.

128. (new) The method of claim 127, wherein said openings are formed in said substrate before said joining said die and said substrate.

129. (new) The method of claim 127, after said joining said die and said substrate, further comprising forming a polymer layer encapsulating said die.

130. (new) The method of claim 127, further comprising forming an adhesive material over said die, followed by said joining said die and said substrate using said adhesive material.

131. (new) The method of claim 127, further comprising forming an adhesive material over said substrate, followed by said joining said die and said substrate using said adhesive material.

132. (new) The method of claim 127, after said joining said die and said substrate, further comprising depositing a conductive material into said openings.

133. (new) The method of claim 132, wherein said conductive material comprises multiple solder balls.

134. (new) A method of forming an electronic package comprising the steps of:

separating a wafer into multiple dies;

after separating said wafer, joining at least one of said dies and a substrate, wherein multiple openings are formed in said substrate and expose said at least one of said dies; and

after said joining said at least one of said dies and said substrate, separating said substrate.

135. (new) The method of claim 134, further comprising depositing a UBM layer over multiple pads formed over an active surface of said wafer, followed by said separating said wafer, followed by said joining said at least one of said dies and said substrate, said UBM layer exposed by said openings in said substrate.

136. (new) The method of claim 134, wherein said openings are formed in said substrate before said joining said at least one of said dies and said substrate.

137. (new) The method of claim 134, wherein said at least one of said dies comprises multiple pads and a passivation layer formed over an active surface thereof, said pads

exposed by said openings in said substrate and exposed by multiple openings in said passivation layer.

138. (new) The method of claim 134, wherein said at least one of said dies comprises multiple first pads, multiple second pads and a passivation layer formed over an active surface thereof, said first pads exposed by said openings in said substrate, said first pads deposited over said passivation layer, multiple openings formed in said passivation layer and exposing said second pads, said first pads electrically connected to said second pads, and said first pads having a layout different from that of said second pads.

139. (new) The method of claim 134, further comprising forming an adhesive material over said substrate, followed by said joining said at least one of said dies and said substrate using said adhesive material.

140. (new) The method of claim 134, after said joining said at least one of said dies and said substrate, further comprising forming a polymer layer encapsulating said at least one of said dies.

141. (new) The method of claim 134, further comprising forming an adhesive material over said wafer, followed by said separating said wafer, followed by said joining said at least one of said dies and said substrate using said adhesive material.

142. (new) The method of claim 141, said depositing said adhesive layer over said wafer is performed using a process comprising spin coating, screen printing or lamination.

143. (new) The method of claim 134, wherein said substrate comprises bismaleimide triazine (BT).

144. (new) The method of claim 134, after said joining said at least one of said dies and said substrate, further comprising depositing a conductive material into said openings.

145. (new) The method of claim 134, wherein said openings are formed using a process comprising mechanical drilling or laser drilling.